A LOW COST 16.2 GHz PHASE LOCKED OSCILLATOR FOR WIRELESS LAN

Thomas A. Bös, Friedbert Bayer*, Urs Lott

Swiss Federal Institute of Technology (ETH) Zürich,
Laboratory for EM Fields and Microwave Electronics
Gloriastr. 35, CH-8092 Zürich, Switzerland, Fax + 41-1-632 11 98
*now with: Bosch Telecom GmbH, Gerberstr. 33, D-71522 Backnang

Abstract

For wireless LAN applications and the wireless ATM network demonstrator system "Magic WAND", a phase locked oscillator was built with standard, low cost components. Although a simple architecture is chosen, the oscillator has a phase noise of -87 dBc/Hz at 10 kHz frequency offset and an output power of 0 dBm at 16.2 GHz. By changing the reference frequency, the output frequency can be tuned from 15.61 GHz to 16.34 GHz without degradation of the phase noise.

Introduction

Wireless local area networks (WLANs) are standardized for a raw data rate up to 2 Mb/s in the ISM frequency band of 2.4 - 2.483 GHz by IEEE 802.11 [1]. For higher data rates, higher transmitting frequencies have to be used due to the limited available bandwidth in the ISM band. Currently different approaches are being investigated, e.g. HIPERLAN and wireless ATM [2]. The phase locked local oscillator described in the paper can be used in the European ACTS project "Wireless ATM Network Demonstrator" (Magic WAND) as signal source for direct downconversion of the 17.1 - 17.3 GHz WLAN band to a 900 MHz IF. It was built with low cost, standard packaged components.

Phase noise of -87 dBc/Hz at 10 kHz frequency offset was measured at 16.2 GHz. The loop bandwidth is 1 MHz and the output power 0 dBm. By changing the reference frequency, the oscillator can be tuned from 15.61 GHz to 16.34 GHz without degradation of the phase noise. Comparable oscillators for the frequency range built for military or radar applications have better phase noise performance, but require more complex architectures and more expensive components [3,4].

Architecture and Components

In Fig. 1 the architecture of the phase locked oscillator is shown with the internal frequencies. The phase locked loop works at 4.05 GHz. Its output is doubled twice to 16.2 GHz. A high reference frequency of 96.43 MHz was chosen to minimize the phase noise degradation by high multiplication

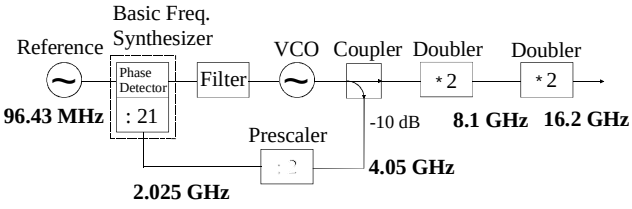

Fig. 1: Architecture of the phase locked oscillator with internal frequencies for 16.2 GHz output

factors. The realization of the architecture with standard commercially available, low cost components is shown in the photographs of Fig. 2 and 3. The circuit is built on two 2" x 2" substrates with an external reference oscillator. The reference oscillator, i.e. a standard TCXO, can still be built on the digital board due to its compact layout.

The digital part, built on a FR4 epoxy (see Fig. 2), consists of a prescaler, frequency synthesizer and loop filter. The GEC Plessy SP8902 prescaler divides the 4 GHz loop frequency by two. The basic PLL frequency synthesizer, Qualcomm Q3236, works up to 2 GHz. The chip includes a phase

0-7803-4603-6/97/$5.00 (c) IEEE

detector and a prescaler. In the loop filter a high speed bipolar operational amplifier, AD847, is used. The passive components are beamlead or SMD devices.

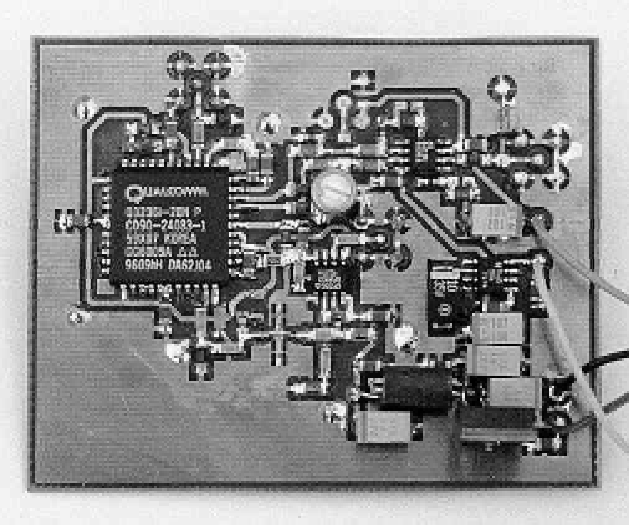

Fig. 2: Photograph of the 2" x 2" substrate including prescaler, frequency synthesizer and loop filter

The high frequency substrate, shown in Fig. 3, is Arlon E10 with a dielectric constant of 10.5 and a thickness of 25 mil. The voltage controlled oscillator, the coupler, the two doublers, all bias and matching networks are integrated. The VCO uses a Si bipolar transistor HP HXTR3675 with a transit frequency f_T = 6 GHz and a varactor diode MA46611D, the only chip component in the design. For both doublers a GaAs field effect transistor Siemens CFY19 with f_T = 12 GHz was used. The passive components on the high frequency substrate are also SMD or beamlead devices.

Design of the VCO and the Doublers

For the simulation of the high frequency building blocks, the voltage controlled oscillator, the coupler and the doublers, the circuit simulator HP EEsof Libra was used. The voltage controlled oscillator was simulated with measured small signal s-parameters. The VCO is of the negative impedance type. The resonator circuit incorporating a varactor diode is connected to the base of the transistor. Shorted stubs at the emitter are designed to maximize the negative impedance seen looking into the base. The well known impedance equations for an oscillator were fulfilled in the linear simulation [5]. The coupler is a simple microstrip parallel line coupler.

For the simulation of the doublers the harmonic balance simulator was used. The FET CFY19 was modeled with a modified Statz model. The package

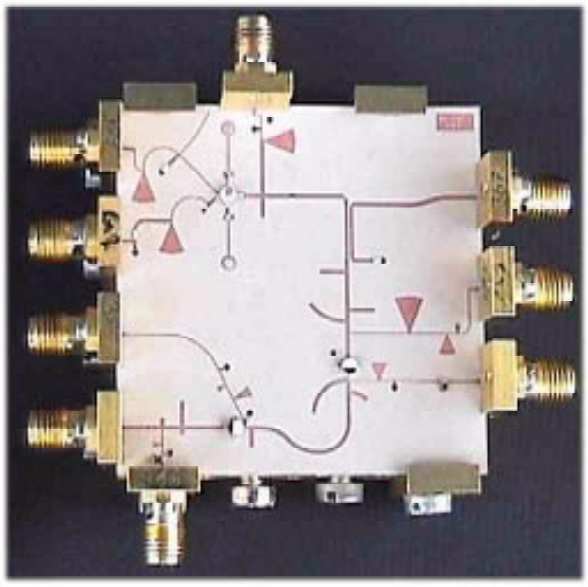

Fig. 3: Photograph of the high frequency 2" x 2" substrate including VCO, coupler and two doublers

parasitics were added to the model with exernal reactive elements. At the drain of the doubler FET, the fundamental frequency f_{in} is reflected by a stub tuned to f_{in}. The phase of the reflection at f_{in} is adjusted by a series transmission line for optimum conversion efficiency [6]. The gate is matched at f_{in} and the drain at $2*f_{in}$.

Measurements

The RF measurements were done with a Spectrum Analyzer HP 8563 E. The reference is a Marconi 2040 low noise signal generator with a phase noise of -140 dBc/Hz at 10 kHz offset frequency (value taken from the user manual). For the single sideband phase noise measurement shown in Fig. 4, an additional low noise preamplifier was used in front

of the spectrum analyzer. At 16.2 GHz phase noise is -87 dBc/Hz at 10 kHz offset. Further measurements showed that the two doublers do not limit the phase noise. The phase noise is only determined by the basic PLL frequency synthesizer. From the data sheet [7] and the total multiplication factor of 168 the phase noise can be calculated as -83.5 dBc/Hz for the chosen architecture. Thus, our particular sample of the basic frequency synthesizer is actually performing 3 ... 4 dB better than specified. With a phase noise improvement of the basic PLL frequency synthesizer chip, the chosen architecture could even have lower phase noise.

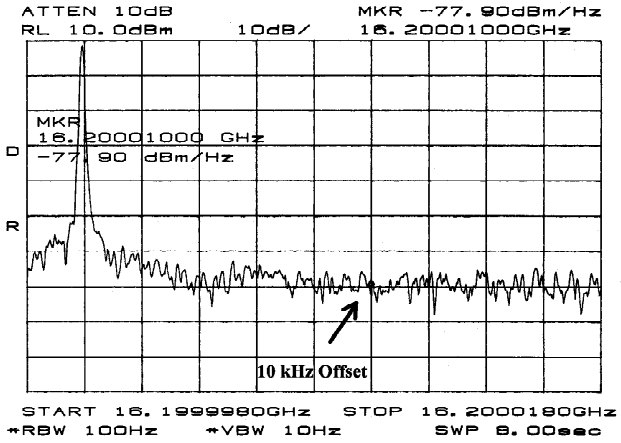

Fig. 4: Single side band phase noise at 10 kHz offset with additional amplification

At 16.2 GHz an output power of 0 dBm was measured with a power meter. The loop bandwidth of 1 MHz can be determined from the spectrum of Fig. 5. With a change of the reference source the frequency of the phase locked signal can be tuned from 15.61 GHz to 16.34 GHz, shown in Fig. 6. Over the tuning range the phase noise characteristic remains constant. Only the output power slightly decreases at frequencies larger than 16.2 GHz. The settling time, which is mainly determined by the loop integrator, was not investigated. In Fig. 7 a plot of the main signal at 16.2 GHz and the unwanted spurious sidebands of the reference, 16.2 GHz ± 96.5 MHz, is shown. The lower spurious sideband at 16.2 GHz - 96.5 MHz is less suppressed than the higher. Still, the lower spurious is suppressed by 42 dB. The subharmonic at 8.1 GHz is only suppressed by 18 dB, because no provision for an additional filter was made.

All components are biased from a single 5 V supply. Only the operational amplifier of the loop filter requires ±5 V and dissipates 60 mW. With 5 V the basic frequency synthesizer and the prescaler dissipate 188 mA of current. The voltage controlled oscillator works at 5 V with 22 mA. The current consumption of each doubler at a supply voltage of only 2.5 V is 15 mA.

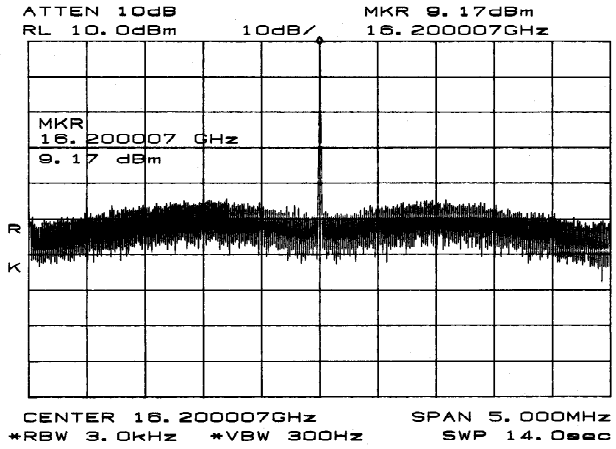

Fig. 5: Measured spectrum for determining the loop bandwidth (with additional amplification)

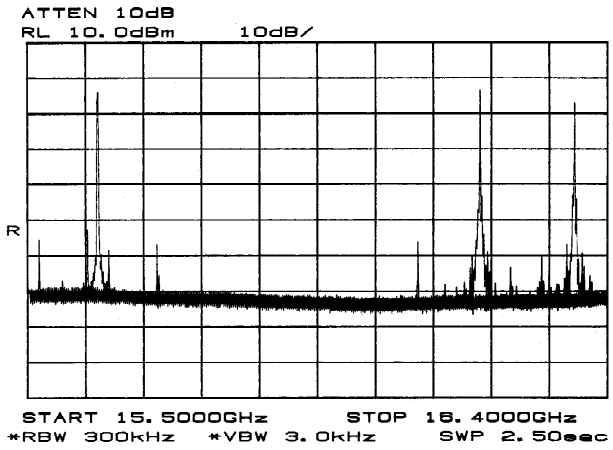

Fig. 6: Tunable frequency range without degradation of the phase noise. Measured oscillator spectra at 15.61, 16.2, 16.34 GHz

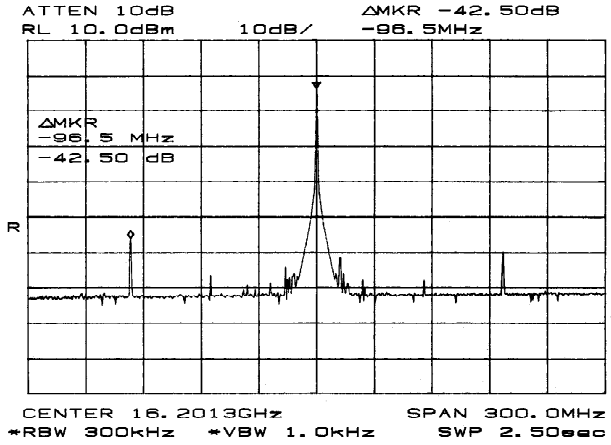

Fig. 7: Unwanted spurious side signals caused by the reference oscillator (16.2 GHz ± 96.5 MHz)

Conclusions

For wireless ATM, i.e. used in the European Magic WAND project, and other wireless LAN applications in the frequency range of 17.1 - 17.3 GHz, a phase locked oscillator was built with low cost, standard packaged components. At 16.2 GHz a phase noise of -87 dBc/Hz at 10 kHz was measured with an output power of 0 dBm. The oscillator can be tuned from 15.61 GHz to 16.34 GHz. The phase noise is limited by the basic synthesizer chip.

Acknowledgment

This work has been performed in the framework of the project ACTS AC085 The Magic WAND, which is partly funded by the European Community and the Swiss BBW (Bundesamt für Bildung und Wissenschaft). The authors would like to acknowledge the contributions of their colleagues from Nokia Mobile Phones, Tampere University of Technology, Technical Research Centre of Finland, Ascom Tech AG, Lucent Technologies WCND, University of Lancaster, Robert BOSCH GmbH, University of Ulm, Compagnie IBM France, IBM Zürich Research Laboratory, ETH Zürich, INTRACOM Hellenic Telecommunications and University of Athens.

References

[1] R.O. LaMaire, A. Krishna, P. Bhagwat, J. Panian, "Wireless LANs and mobile networking: standards and future directions", IEEE Communications Magazine, August 1996, pp. 86 - 94

[2] B. Walke, D. Petras, D. Plassmann, "Wireless ATM: Air interface and network protocols of the mobile broadband system", IEEE Personal Communications, August 1996, pp. 50 - 56

[3] W. Konrath, "Fully integrated 18 - 20 GHz phaselocked DRO signal source for digital radio systems using chip & wire technology", 21st European Microwave Conference, Stuttgart 1992, pp. 1359 - 1364

[4] T. Ohira, H. Kato, K. Araki, F. Ishitsuka, "A compact full MMIC module for Ku-band phase-locked oscillators", IEEE Trans. on MTT, vol.37, No. 4, April 1989, pp. 723 - 728

[5] K. Chang, "Microwave solid state circuits and applications", John Wiley & Sons, 1994

[6] C. Rauscher, "High-frequency doubler operation of GaAs field-effect transistors", IEEE Trans. on MTT, vol.31, No. 6, June 1983, pp. 462 - 473

[7] Qualcomm Q3236, 2.0 GHz low power PLL frequency synthesizer, Technical Data Sheet, February 1996